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13. ABSTRACT *(Maximum 200 words)*

The devices used in the military need to be of high voltage, high temperature and high frequency. Silicon Carbide is a suitable material for the development of such materials. Power Semiconductor Research Center is a leader in this research area to use Silicon Carbide. Simulation results showed that Lateral RESURF MOSFETs with breakdown voltage up to 1600 volts can be made. The behavior of RESURF devices are provided. The overview of RESURF diode and MOSFETs are given. Process techniques are also provided.

In order to fabricate 4H-Silicon Carbide Lateral N-Channel MOSFETs, P-Channel MOSFETs in a thin active Silicon Carbide layer formed on top of a high resistivity isolation layer, Hydrogen and Helium can be used to produce deep layer traps.

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RESURF, Gauss's Law, Silicon Carbide, Oxide Rupture Filed, Dielectric Constant, Electric Field Profile, Nitride MOSFETs, Diode, N-Channel, P-Channel, Isolation layer, Lateral.

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High Voltage 4H-SiC Lateral RESURF Devices

S. Sonkusale, A.Venkateswaran, P.Mehrotra and B.J Baliga

Abstract

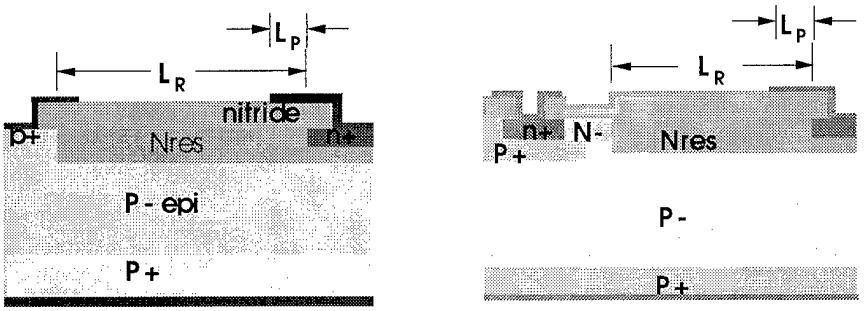
Silicon Carbide is an attractive material for development of high voltage, high temperature and high frequency devices .SiC has the critical field ten times higher than that of silicon. This implies that Lateral RESURF devices made in SiC can support the same breakdown voltage in a much smaller drift length as compared to the silicon devices. In our project we are using the concept of Lateral RESURF device to obtain diodes and MOSFET having high breakdown voltages greater than 1800 volts and small specific on resistance. In this report we have provided briefly the behavior of RESURF devices with varying RESURF dose .It gives the overview of design of RESURF diode and MOSFET and the various parameters that we have changed in these devices while fabrication.

The report gives more emphasis on the process technique used in fabrication done till present.

Introduction:

The goal of this project is to develop ICs that work in the same environment as high power devices . To achieve this goal we have applied RESURF principal to get high voltage device in SiC. Supporting high voltages in lateral SiC power devices requires a uniform lateral electric field in the drift region in accordance with the RESURF (REduced SURFace electric field principle). RESURF prevents electric field at the surface in lateral devices from reaching critical value and hence reducing the surface breakdown. In this project we have done extensive simulation to find out the optimum dose of RESURF layer .Currently we are fabricating the lateral RESURF single zone accumulation MOSFET and diode with different RESURF dose.

RESURF DIODE & RESURF MOSFET



RESURF Diode **RESURF MOSFET**

N_{res}: RESURF Layer Dose- RESURF depends on charge in the RESURF layer

L_R: RESURF Layer Length - Minimum length to get maximum BV

L_P: Field Plate Length - BV can be affected by electric field profile at drain/cathode end

We are varying RESURF layer dose, RESURF layer length and field plate length in our devices .The parameters chosen are given in device design matrix

Device Analysis and Design:

Device Design Matrix

No.	L_R (u)	L_P (u)
1	5	3
2	10	3
3	15	3
4	20	3
5	25	1
6	25	2
7	25	3
8	25	4
9	30	3

Lateral RESURF Diodes

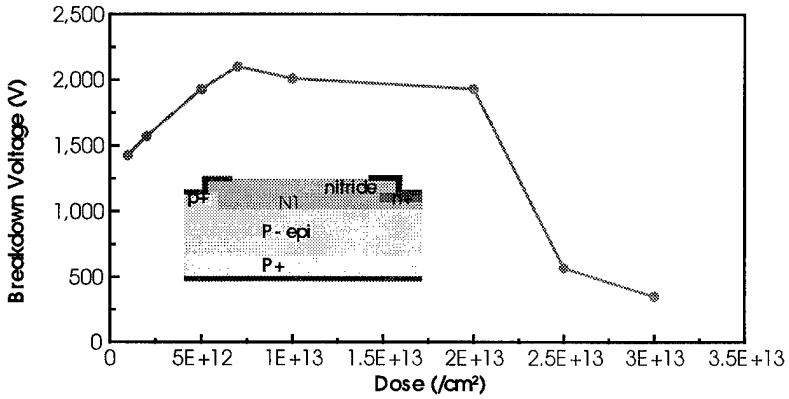
No.	L_R (u)	L_P (u)
1	10	3
2	15	3
3	20	3
4	25	2
5	25	3
6	25	4
7	30	3
8	35	3

Lateral RESURF MOSFETs

In the previous studies ,we have done numerical simulation on RESURF devices ,which included diodes and lateral MOSFETs .It was observed at the optimum dose of RESURF layer we have comparable electric field at the anode and cathode in diodes, and at source and drain in lateral MOSFET. At these optimum doses we get highest breakdown voltages. The electric field produced at such high breakdown voltages may cause oxide rupture. Hence we also studied the effect of using nitride which has lower dielectric constant. For 4H-SiC MOSFET ,breakdown voltage(>1800 V) were obtained for a wide range of RESURF doses (3e12/cm^2 - 1e13/cm^2).The optimum dose for 4H-SiC MOSFET is 5-10X higher than for Silicon devices. For diodes high breakdown voltages (>2000 V) were obtained for the RESURF dose (7e12/cm^2 - 2e13/cm^2).The optimum dose for diodes is 10-20 X higher than Silicon devices

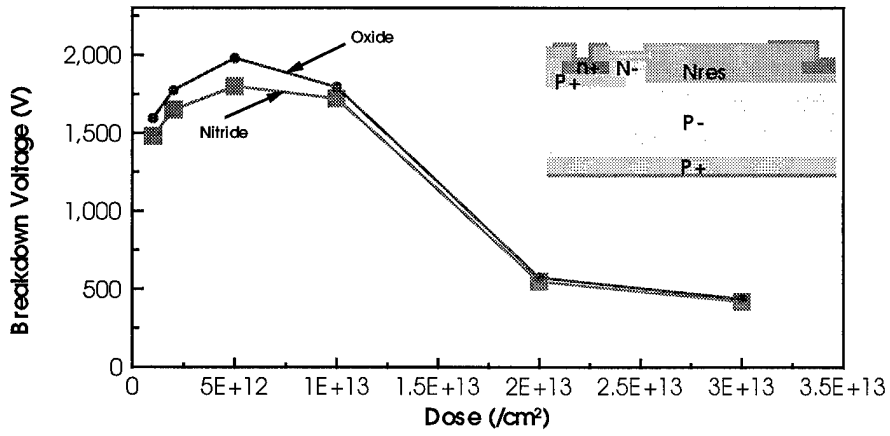
Based upon this mask set was designed with various RESURF length to provide experimental verification. A mask layout (using 2 micron design rules) was performed with an array of diodes and MOSFETS (both inversion and accumulation type) using the layout editor LTL. In addition ,various diagnostic test elements have been included to help determine different properties. These include Hall elements for mobilities, Van der Pauw structures for sheet resistance ,TLM structures for contact resistances and capacitors .Apart from these some aggressive designs using stricter design rules have been added. The process uses 11 masks in all. The first run has only single zone RESURF devices.

Breakdown Voltage vs Dose for single zone RESURF diode with nitride as dielectric

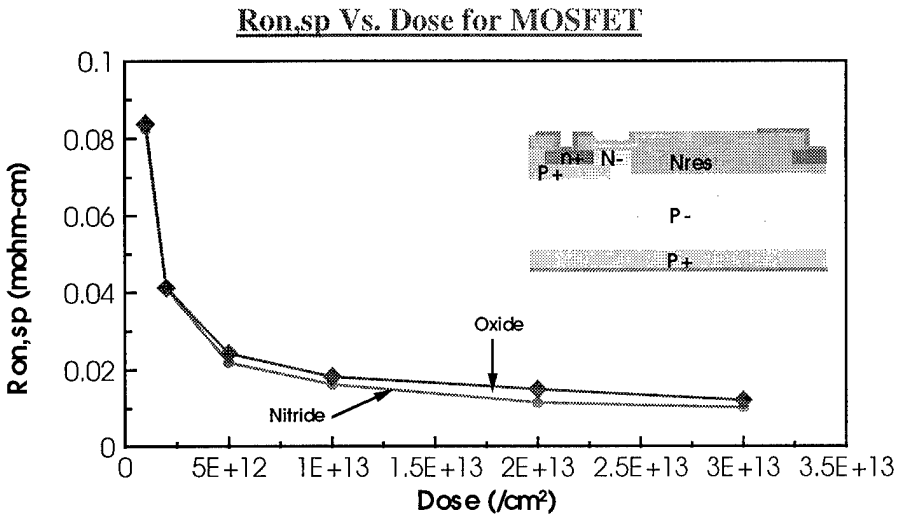


- Maximum Breakdown voltage (2100 V) at dose of 7e12/cm^2
- High BV obtained for doses as high as 2e13/cm^2
- The optimum dose is an order of magnitude higher than that in Si

BV Vs. Dose for MOSFET



In lateral RESURF MOSFET we find that breakdown voltage is less if we use nitride as dielectric instead of oxide. Specific on-resistance is also less if we use nitride and the device are more reliable at high voltages.



Process flow and Device fabrication :

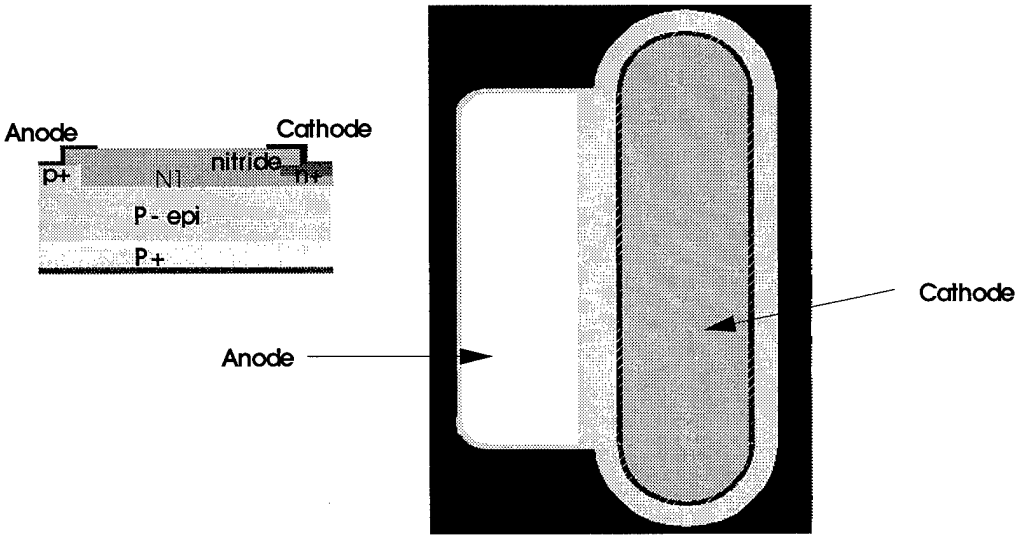
A process flow for RESURF was designed .The implant doses and thickness of the oxide used as masks for implants were determined by the careful analysis of simulation results. In September 2000,the processing was assigned to Sachin Sonkusale, Research Assistant at Power Semiconductor Research Center. The process is at 6th mask level this time.

Process flow and Device fabrication (detailed update)

Four 4H-SiC wafers are used to fabricate diodes and MOSFETS with eight different RESURF doses. The wafers are cleaned and patterned using first mask. The wafers were then RIE etched using 0.25-0.3 microns SiC trench etch recipe. This was done to produce the alignment marks on the wafers. After stripping resist ,wafers were again cleaned and LTO deposition of about 1.6 microns was done. The wafers were patterned using the second mask. The oxide was etched to a depth of 1.3 microns using an RIE process. The remaining oxide was removed in BOE solution. The resist was then removed and wafers cleaned . The wafers were then sent out for the p+ buried implant (Boron Dose=1e14 cm^{-2} ,Energy 380 keV, Temp=1000 ^{o}C Angle=0^{o}, front side).

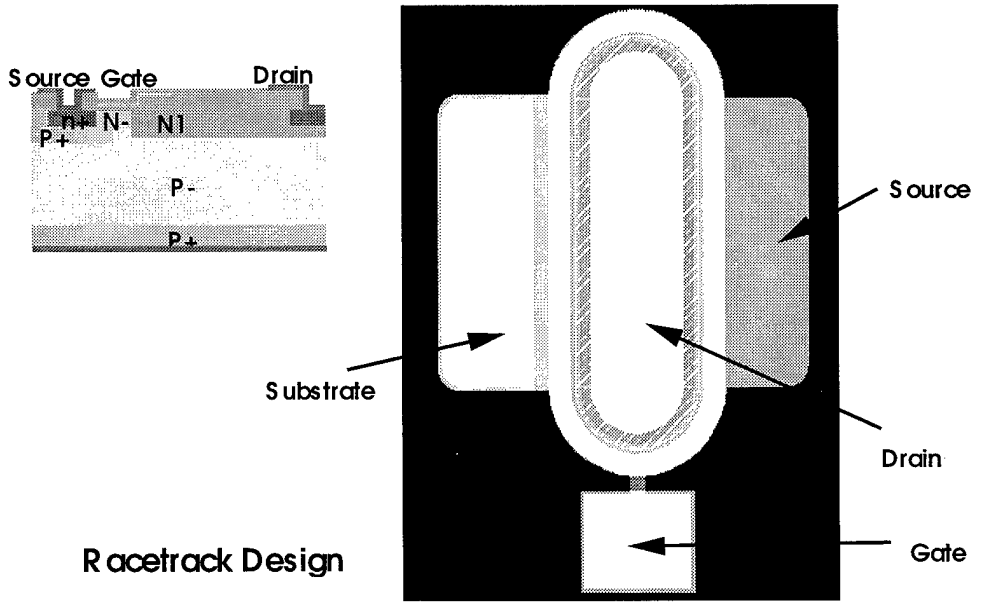
After the implant ,the oxide mask was stripped in BOE solution and cleaned in the preparation for the next layer. LTO oxide of about 1.0 microns thick is deposited on our wafers, which is patterned using the third mask. The oxide is etched in a BOE solution .The resist is stripped and wafers cleaned .The wafers are then sent for p+ sinker implant (Aluminum dose=4e15 cm^{-2} Energy 25 keV ,1e15 cm^{-2} Energy 75keV, 8e14 cm^{-2} Energy 250 keV, Temp=1000 ^{o}C , Angle=0^{o} front side).We use multiple ion implants to get near constant dopant profile for p+ sinker.

Layout of the Single Zone RESURF Diode



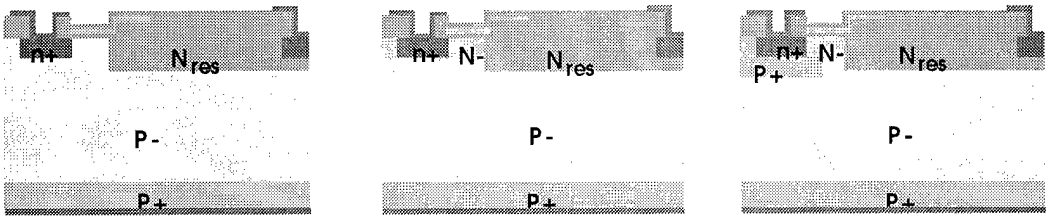
Racetrack Design

Layout of the Single Zone RESURF MOSFET



Racetrack Design

PROCESS FLOW



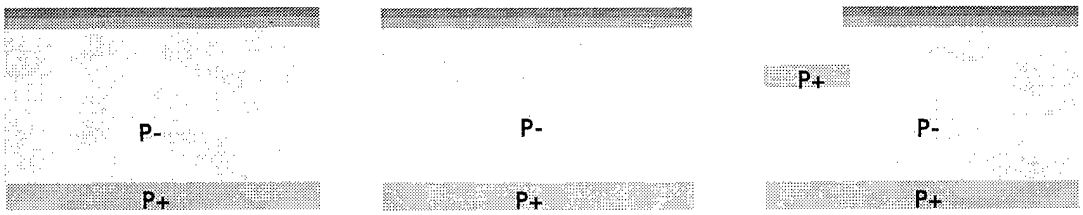
Single Zone RESURF MOSFETs

1st Mask

- Ist mask used to etch alignment marks on wafers

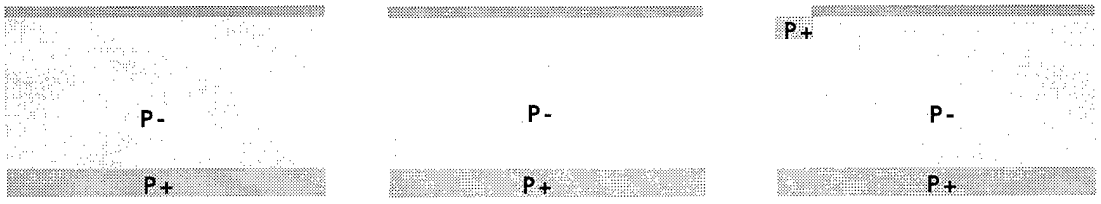
2nd Mask

- Use the second Mask to pattern the oxide and ploy
- Implant B to make p+ deep implant (Hot implant)



3rd Mask

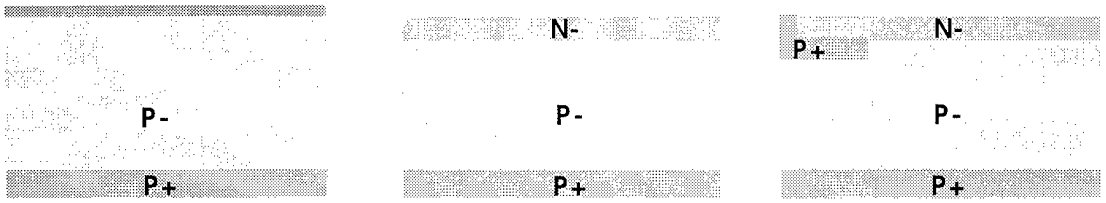
- Pattern oxide to make shallow p+ implant (hot implant)



After implant the oxide mask was then stripped in a BOE and cleaned for preparing next layer. LTO oxide of 1.0 microns is deposited on our wafers and patterned using mask 4. The oxide was etched to a depth of 0.8 microns using RIE process. The remaining oxide was removed in BOE solution. The resist was stripped and wafers cleaned .The wafers were sent out for the N- implant (Nitrogen dose of 5e11 cm^{-2} ,Energy 150 keV, Temp=1000 ^{o}C ,Angle=0^{o} , front side)

4th Mask

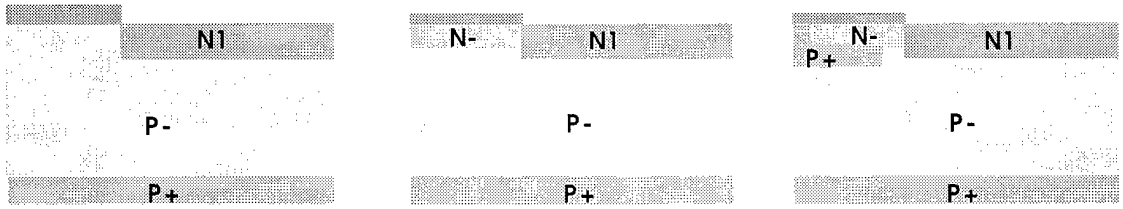
- Pattern oxide using 4th mask
- Implant nitrogen (hot implant) to make n- base layer



The next layer was done using the same steps and mask 5 .the implants were then done according to wafer split.

5th Mask

- Pattern oxide using 5th mask for first resurf implant
- Implant nitrogen (hot implant) to make the resurf layer



Wafers split for the first run :

- One half of each wafer got 1 RESURF dose
- During implantation one half of the wafer was covered and the other half was again implanted with the same dose X
- Next, the entire wafer was again implanted with the same dose X.

This process gives us two different resurf doses on the same wafer .The dose on one half of the wafer is double that of the dose in other half of the wafer

Wafers split for the first run :

Wafer No.	Dose in 1st half (/cm^2)	Dose in 2nd half (/cm^2)
1	1e12	2e12
2	3e12	6e12
3	8e12	1.6e13
4	2e13	4e13

Future Plans :

The fabrication of these devices is scheduled to complete before April 2001.After that the device will be characterized for the evaluation of their breakdown strength, specific on-resistance. Other important parameters such as sheet resistance, mobilities of carriers, contact resistance and capacitors will also be measured.

Acknowledgements:

The authors would like to thank the sponsors of the Power Semiconductor Research center and ONR for supporting this work and Avanti for providing simulation software.

References

1. Ravi Kiran Chilukuri and Dr. B.J.Baliga ,"High Voltage 4H-SiC ACCUFETs", Ph.D. dissertation 2000.
2. Srikant Sridevan and Dr. B.J.Baliga, Characterization of Inversion Layers in SiC", Ph.D. dissertation 1998.

PROPERTIES OF 4H-SiC IMPLANTED ISOLATION LAYERS

P.R.Singh, S.Venkatesan, B.J.Baliga

Abstract

In SiC ICs vertical isolation may be required because of high voltages. SiC with deep level traps provide high resistivity. By implantation of neutral species these deep level traps can be generated and vertical isolation can be provided. The objective of this research is to fabricate N-channel MOSFETs and P-channel MOSFETs on top of a high resistivity isolation layer. Simulations of SiC with deep level traps are performed. Schottky diodes as well as MOSFETs with isolation layer are simulated. It has been found that the required isolation layer can be formed by ion implantation of H and He. It has also been found that these devices are isolated at least up to 100 V.

A. **Introduction**

If we are to develop ICs for SiC, lateral isolation may not be sufficient as in the Si ICs. The working voltage is high for these devices, so the devices will interfere more with each other. For these devices it will be better if we are able to provide vertical isolation. It will be possible to incorporate vertical devices as well as lateral devices in the ICs. The objective of this research is to fabricate 4H-SiC lateral N-channel MOSFETs, P-channel MOSFETs in a thin active SiC layer formed on top of a high resistivity isolation layer. The isolation layer will be formed by ion implantation of neutral ions, such as Hydrogen, helium, carbon to produce deep level traps. As a initial step towards the device fabrication, schottky diodes will be fabricated and the characteristics will be evaluated using the I-V plot, these diodes will be used for finding the trap level using Deep Level Transient Spectroscopy (DLTS). Based on the performance characteristics of this initial diode the MOSFETs will be fabricated. The fabricated MOSFETs will also be tested for their electrical characteristics and the effect of the isolation layer.

B. **Simulations**

Extensive 2-dimensional simulations were performed using MEDICI. Simulations were done to determine the resistivity change when a donor level trap is introduced at midgap. The resistivity, hole and electron concentration were determined with change in trap concentration. The concentration of the traps was changed over range 1e10 to 1e20 cm^{-3}. It is found that resistivity is maximum when the trap concentration is between 1e16 to 2e16 cm^{-3}. The maximum resistivity is found to be 1.05e22 ohm-cm at 1.5e16cm^{-3} trap concentration. This resistivity is high enough to provide isolation.

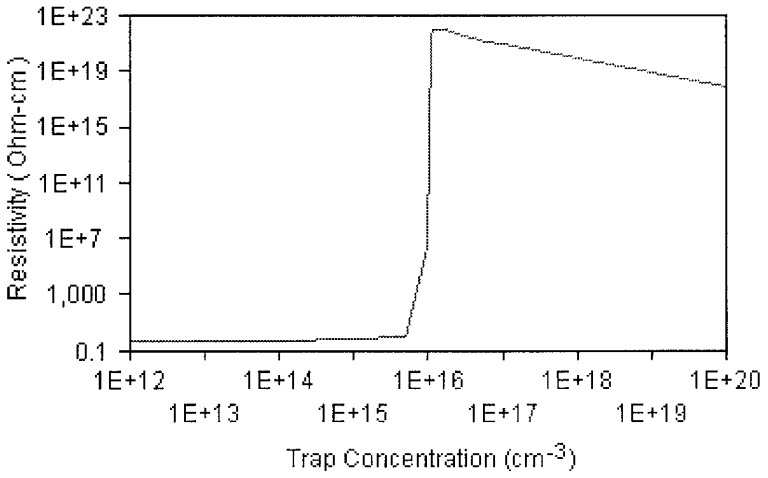


Fig.1 Resistivity vs trap concentration

To test the properties of the high resistivity layer schottky diodes with isolation layer are to be simulated and fabricated. For the schottky diode, the 4H-SiC epitaxial layer is p-type ($1x10^{16}$ cm^{-3}, aluminum doped)

on p+ substrate and is 10 μm thick. The forward voltage drop of the schottky diode is given by-

$$V_F = \frac{\eta kT}{q} \ln\left(\frac{J_F}{A^* T}\right) + \eta\Phi_{bn} + R_{s,sp}J_F$$

Where k is Boltzman's constant, η is ideality factor, J_F is current density, A^* is the effective Richardson's constant, Φ_{bn} is the barrier height, and $R_{s,sp}$ is the specific series resistance. The contact metal is defined to have barrier height of 1.4 eV as reported for 4H-SiC and Titanium/Aluminum contact [1]. The I-V plot of the schottky diode is given in figure 3(a). To study the effect of deep level traps, donor type midgap material is inserted as given in figure 2. The profile of the traps is taken to be gaussian as they are to be implanted. The characteristic length of the gaussian distribution is taken to be that of Helium implant. The simulations were performed for 0.5 μm to 1.5 μm depth of the peak trap concentration. To vary the thickness of the layer two trap profiles separated by small distance is simulated. The peak concentration of the traps is varied from 1e17 to 1e19 cm^{-3}. The I-V curve for a typical schottky diode with isolation layer is given in figure 3(b). The layer provides good isolation up to several hundreds of volts. The simulation results imply that this layer can be used as isolation. As SiC devices are used for power applications, the simulation were performed up to 500 K and isolation is found to perform satisfactorily.

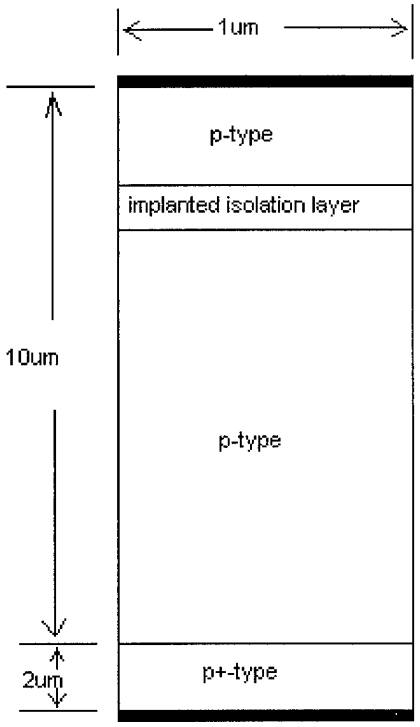


Fig 2. Schottky diode with isolation layer

Fig 3 (a)

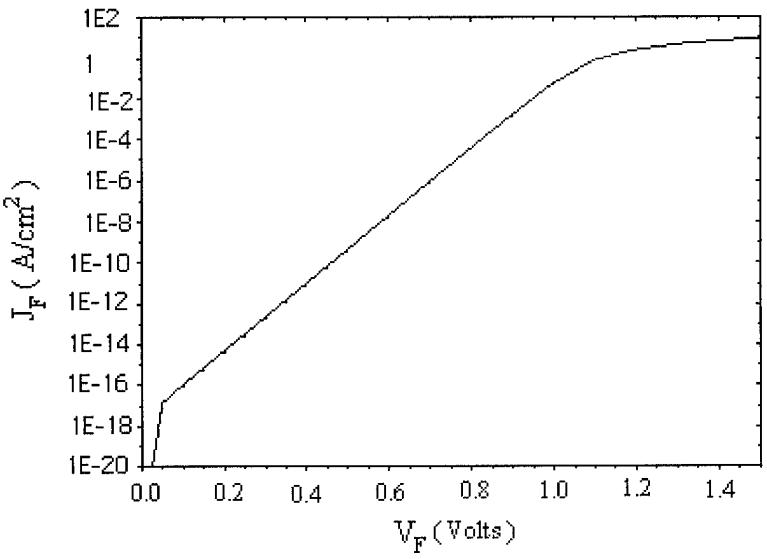


Fig 3 (b)

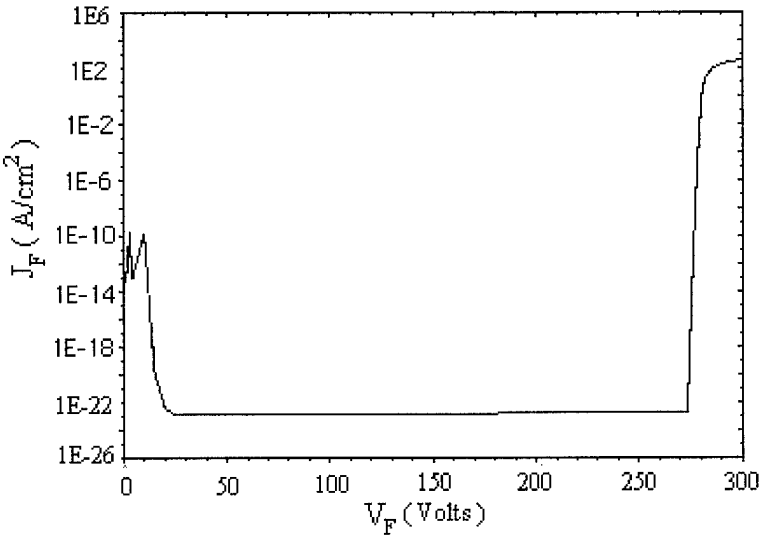


Fig 3. J_F vs V_F curves for (a) Schottky diode (b) Schottky diode with isolation layer

MEDICI simulations were performed for N-channel MOSFET and P-channel MOSFET also. The structure used for N-channel MOSFET is given in figure 4. The gate length is 2μm and the depth of the source and drain is 0.1μm. It is found that if isolation layer is not sufficiently deep from the surface then it affects the operation of MOSFET. It is found for given structure that if the isolation layer is more than 1.0 μm deep it does not affect the MOSFET. The layer provides good isolation of the MOSFET from the back contact for at least up to 100V.

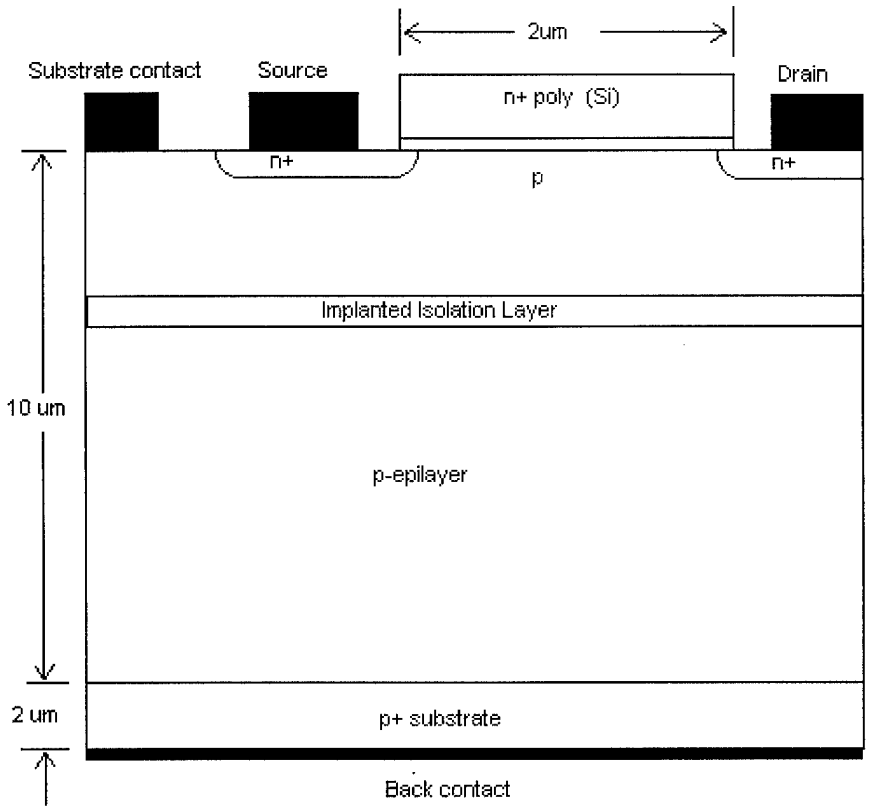


Fig.4 Structure for N-channel MOSFET on top of the isolation layer

TSUPREM4 simulations were performed to find the implantation energy, dose of the implant to form isolation layer. It is found that given the maximum energy of 200keV only lighter species, H^+ and He^+, can give required depth.

C. Fabrication

On the basis of simulations, schottky diodes are to be fabricated with implanted layers to test the concept. The four test implantations are:

1. H^+ ion implantation at 200 keV with dose 1e15 cm^{-2},
2. H^+ ion implantation at 200 keV with dose 1e15 cm^{-2} and at 160 keV with dose 1e15 cm^{-2},
3. H^+ ion implantation at 200 keV with dose1e16 cm^{-2},
4. He^+ ion implantation at 200 keV with dose 1e16 cm^{-2}.

The above implantation has been done. Presently the fabrication of the diode is being done.

D. Conclusion

In conclusion, from the simulations it has been demonstrated that the MOSFETs can be fabricated on top of an isolation layer. The required depth for isolation layer for the designed device has to be more then 1.0 μm. The isolation layer can be formed using ion implantation of lighter species like H or He. The layer provides isolation at least up to 100 V.

Acknowledgment

The authors wish to thank the ONR for supporting this work. The authors also wish to thank *Avanti* for providing simulation software.

References

1. R.Raghunathan and B.J.Baliga," p-type 4H and 6H-SiC High-voltage schottky barrier diodes," IEEE Electron Device Letters, vol. 19, pp.71-73, March 1998.
2. Dev Alok, PhD Thesis, NC State University, 1996